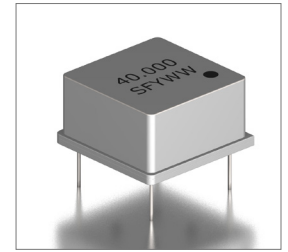


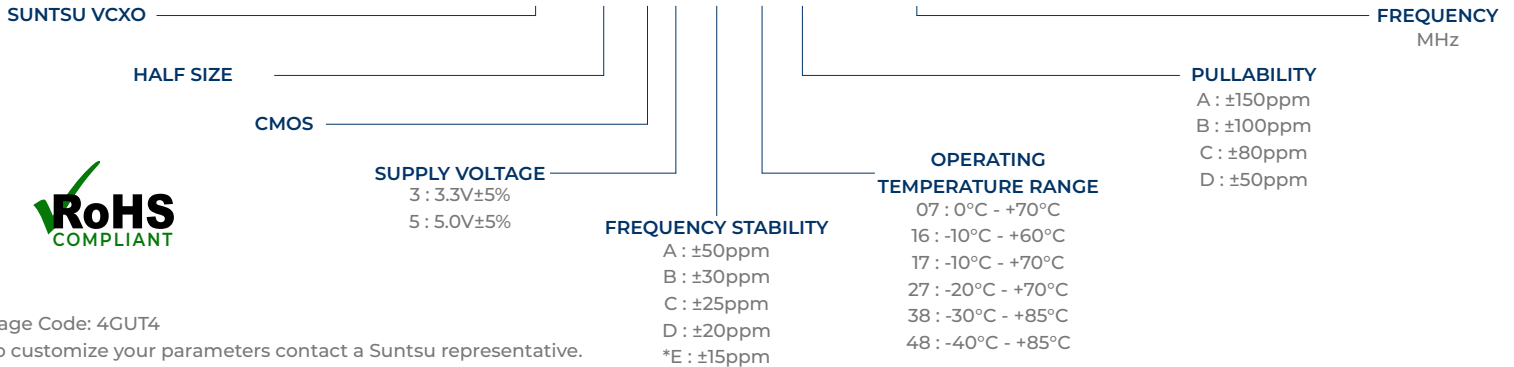
| Features |
|---|
| <ul style="list-style-type: none"> ±20ppm (Frequency Stability) Available Standard Half Size Package CMOS/TTL Compatible Fundamental or PLL (Phase Lock Loop) Available |

| Applications |
|---|
| <ul style="list-style-type: none"> Phase Locked Loops Circuit Synthesizers Base Stations |



Part Numbering Guide

SVC HS C 3 A 48 A - 40.000M



Cage Code: 4GUT4

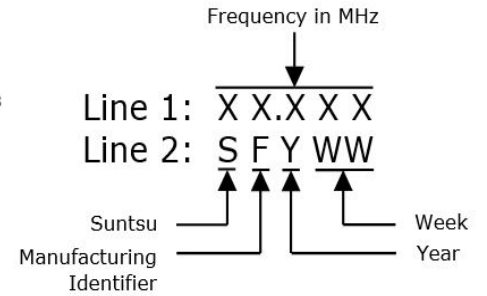
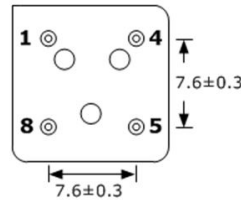
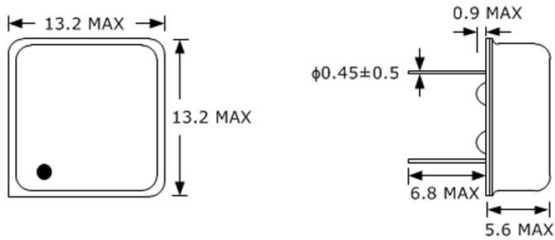
To customize your parameters contact a Suntsu representative.

* For frequency stability option E contact a Suntsu representative.

| Electrical Parameters | Units | Minimum | Typical | Maximum | Remarks |
|--|-------|---------------------|---------|---------------------|---------------------------------------|
| Frequency Range | MHz | 1 | | 160 | |
| Frequency Stability (Includes Initial Tolerance at 25°C, Frequency Stability over Operating Temperature, Output Load Change, Supply Voltage Change, and First Year Aging at 25°C.) | ppm | -20 | | +20 | See part numbering guide for options. |
| Operating Temperature | °C | -40 | | +85 | See part numbering guide for options. |
| Storage Temperature | °C | -55 | | +125 | |
| Supply Voltage (V _{DD}) 3.3V Option | V | 3.135 | 3.3 | 3.465 | |
| Supply Voltage (V _{DD}) 5.0V Option | V | 4.750 | 5.0 | 5.250 | |
| Current (I _{DD}) 3.3V Option | mA | | | 40 | |
| Current (I _{DD}) 5.0V Option | mA | | | 50 | |
| Current Voltage (V _C) 3.3V Option | V | 0.3 | | 3.0 | |
| Current Voltage (V _C) 5.0V Option | V | 0.5 | | 4.5 | |
| Pullability | ppm | ±50 | ±100 | ±150 | See part numbering guide for options. |
| Linearity | % | | | 10 | |
| Output Load (CMOS) | pF | | | 15 | |
| Output Load (TTL) | TTL | | | 10 | |
| CMOS Output Logic HIGH (V _{OH}) | V | 0.9*V _{DD} | | | |
| CMOS Output Logic LOW (V _{OL}) | V | | | 0.1*V _{DD} | |
| TTL Output Logic HIGH (V _{OH}) | V | 2.4 | | | |
| TTL Output Logic LOW (V _{OL}) | V | | | 0.4 | |
| Rise (T _r) And Fall (T _f) Time | ns | | | 5 | |
| Symmetry (Duty Cycle) | % | 45 | 50 | 55 | |
| Start-Up Time | ms | | | 10 | |
| Phase Jitter (12KHz ~ 20MHz) | ps | | | 1 | AT-Cut Fundamental |
| Phase Jitter (12KHz ~ 20MHz) | ps | | | 5 | PLL (Phase Lock Loop) |

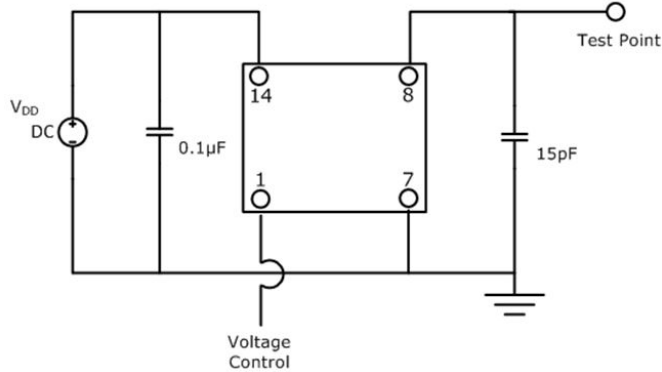
Outline Drawing & Part Marking

All dimensions are in millimeters (mm) unless otherwise noted. Drawings are not to scale.

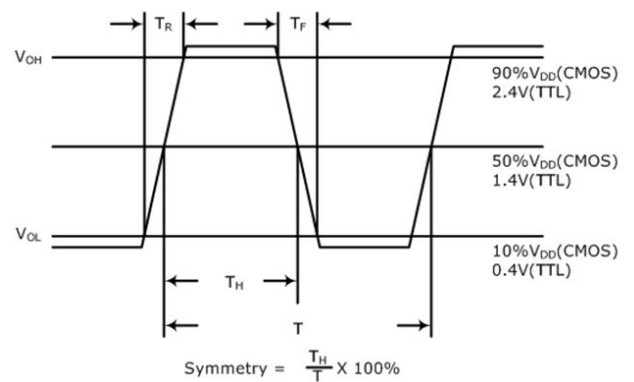


| PIN | FUNCTION |
|-----|-----------------|
| 1 | VOLTAGE CONTROL |
| 4 | GND |
| 5 | OUTPUT |
| 8 | V _{DD} |

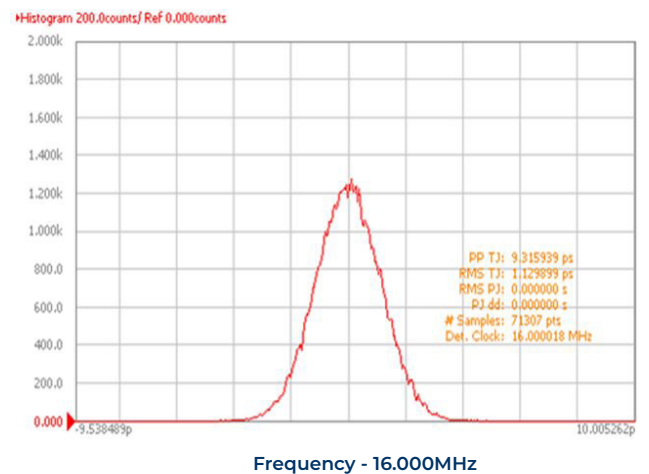
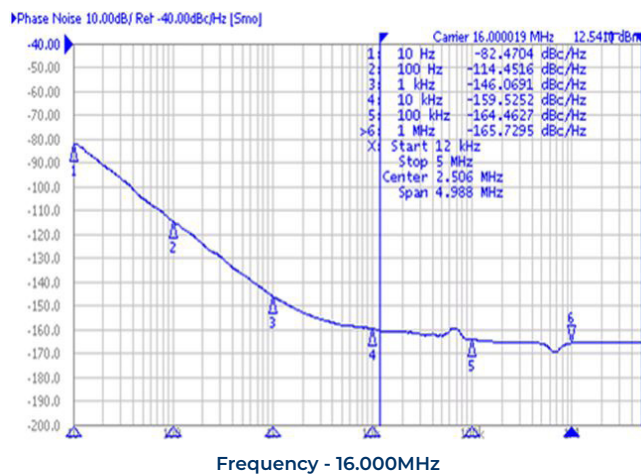
Test Circuit (CMOS/TTL Compatible)



Waveform (CMOS/TTL Compatible)



Typical Phase Noise and Jitter Performance (Measured By Agilent E5052A)



| Environmental Specifications | | Mechanical Specifications | |
|------------------------------|---------------------------------------|------------------------------|---------------------------------------|
| Temperature Cycling | MIL-STD-883, Method 1010, Condition B | Mechanical Shock | MIL-STD-202, Method 213, Condition B |
| Fine Leak Test | MIL-STD-883, Method 1014, Condition A | Vibration | MIL-STD-883, Method 2007, Condition A |
| Gross Leak Test | MIL-STD-883, Method 1014, Condition C | Moisture Resistance | MIL-STD-883, Method 1004 |
| Solderability | MIL-STD-883, Method 2003 | Resistance to Solvents | MIL-STD-202, Method 215 |
| Moisture Sensitivity | J-STD-020, MSL 1 | Resistance to Soldering Heat | MIL-STD-202, Method 210, Condition K |